Delta-sigma ADCs in a nutshell

Part one of a three-part series exploring the basic topology and functions of delta-sigma ADCs.
By Bonnie Baker -- EDN, 12/14/2007

Delta-sigma converters are ideal for converting signals over a wide range of frequencies from dc to several megahertz with very-high-resolution results. **Figure 1** shows the basic topology, or core, of a delta-sigma ADC, which has an internal delta-sigma modulator in series with a digital filter. As you explore delta-sigma ADCs, you will find that, although they have a variety of other features, they all possess this basic structure. This column and the next three *Baker's Best* columns explore the basic topology and functions of these two modules.

The input signal to the delta-sigma ADC is an ac or dc voltage. This and the next three *Baker's Best* columns use a single cycle of a sine wave as the input signal. Using a 1-bit internal ADC, the internal converter modulator in **Figure 1** samples the input signal, producing a coarse, quantized output. The modulator converts the analog-input signal into a high-speed, pulse-wave representation. The ratio of ones to zeros in the modulator's output pulse train mirrors the input-analog voltage. Although the modulator produces a noisy output, future columns will show that the circuit "shapes" this noise into the higher frequencies of the output spectrum. This action paves the way for a low-noise, high-resolution conversion at the output of the digital filter.

At the modulator output, the digital filter addresses high-frequency noise and high-speed-sample-rate issues. Because the signal now resides in the digital domain, you can apply a lowpass digital filter to attenuate the higher frequency noise and a decimator filter to slow down the output-data rate. The digital/decimator filter samples and filters the modulator's stream of 1-bit codes and creates a slower multibit code.

Although most converters have only one sample rate, delta-sigma converters have two: the input sampling rate and the output-data rate. The ratio of these two meaningful variables defines the system's decimation ratio. A strong relationship exists between the decimation ratio and the converter's effective resolution. A future column will examine how the modulator, digital/decimator filter, and adjustable decimation ratio work.

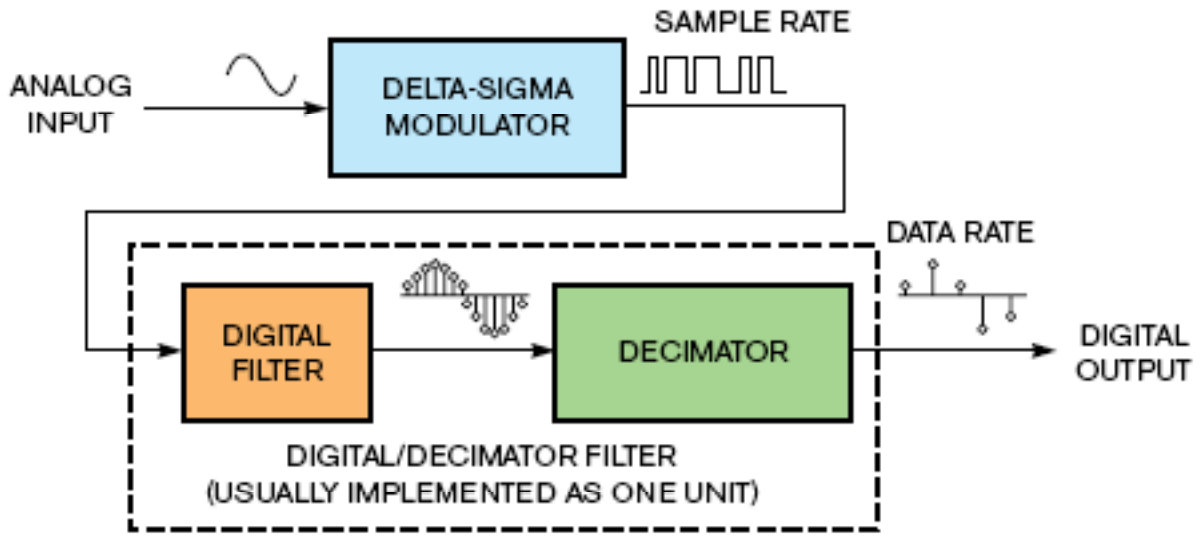

Figure 1 The core functions inside any delta-sigma ADC are a delta-sigma modulator and a digital/decimator filter.

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Reference
1 Baker, R Jacob, *CMOS Mixed-Signal Circuit Design: Volume II*, John Wiley & Sons, 2002, ISBN: 0471227544.

Delta-sigma ADCs in a nutshell, part 2: the modulator

Unlike most quantizers, the delta-sigma modulator includes an integrator that shapes the quantization noise.

By Bonnie Baker -- EDN, 1/17/2008

A delta-sigma converter uses many samples from the modulator to produce a stream of 1-bit codes. The delta-sigma ADC accomplishes this task by using an input-signal quantizer running at a high sample rate. Like all quantizers, the delta-sigma modulator takes an input and produces a stream of digital values that represents the voltage of the input. You can look at the delta-sigma modulator in the time or in the frequency domain. If you look at a time-domain representation, you can see the mechanics of a first-order modulator (**Figure 1**).

The modulator measures the difference between the analog-input signal and the analog output of a feedback DAC. An integrator then measures the analog-voltage output of the summing junction and presents a sloping signal to the 1-bit ADC. The 1-bit ADC converts the integrator's output signal to a digital one or zero. Using the system clock, the ADC sends the 1-bit digital signal to the modulator's output, as well as back through the feedback loop, where a 1-bit DAC is waiting.

The 1-bit ADC digitizes the signal to a coarse output code that has the quantization noise (e_i) of the converter. The modulator output is equal to the input plus the quantization noise, (e_i–$e_{i–1}$). As this formula shows, the quantization noise is the difference of the current error (e_i) minus the previous error ($e_{i–1}$) of the modulator. The time-domain output signal is a pulse-wave representation of the input signal at the sampling frequency, f_S. If you average the output-pulse train, it equals the value of the input signal.

The frequency-domain diagram tells a different story (**Figure 2**). The time-domain output pulses in the frequency domain appear as the input signal (or spur) and shaped noise. The noise characteristic in **Figure 2** is the key to the modulator's frequency operation.

Unlike most quantizers, the delta-sigma modulator includes an integrator that shapes the quantization noise. The noise spectrum at the modulator output is not flat. More important, in a frequency analysis, you can see how the modulator shapes the noise to higher frequencies, facilitating the production of a higher resolution result.

The modulator output in **Figure 2** shows that the quantization noise of the modulator starts low at 0 Hz, rises rapidly, and then levels off at a maximum value at the modulator sampling frequency.

Integrating twice with a second-order modulator, instead of just once, is a great way to minimize low-frequency quantization noise. Most delta-sigma modulators are of a higher order. For instance,

the designs of the more popular delta-sigma converters include second-, third-, fourth-, fifth, or sixth-order modulators. Multi-order modulators shape the quantization noise even harder to higher frequencies.

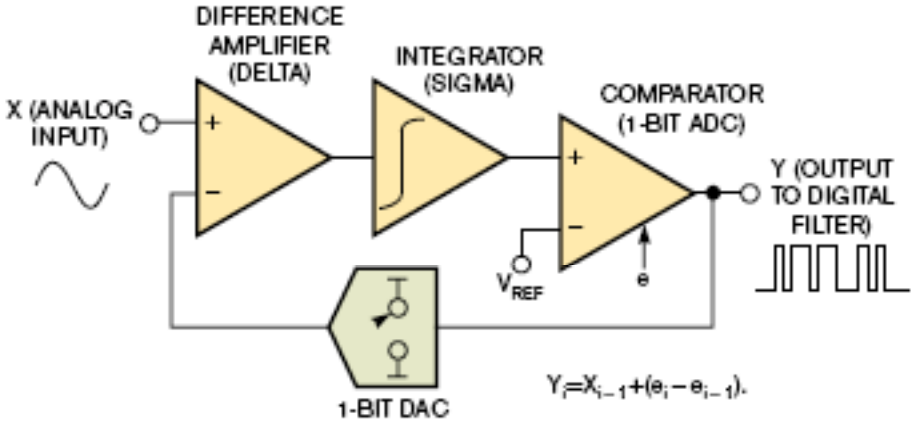

Figure 1 A time-domain representation shows the mechanics of a first-order modulator.

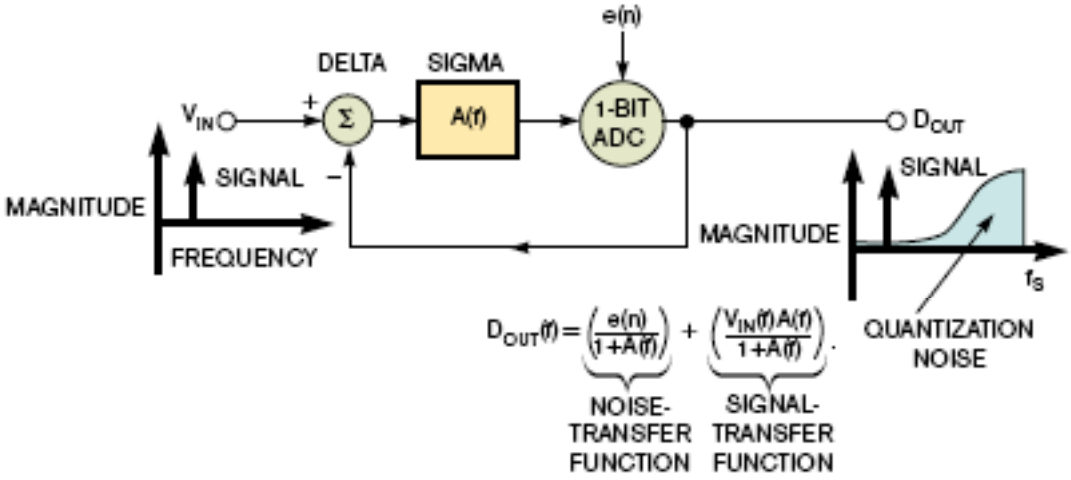

Figure 2 In a frequency-domain representation, the noise characteristic is key to the modulator's frequency operation.

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References

1. Baker, Bonnie, "**Delta-sigma ADCs in a nutshell**," *EDN*, Dec 14, 2007, pg 22.
2. Baker, RJ, *CMOS mixed-signal circuit design*, Wiley & Sons, ISBN 0471227544, May 2002.

Delta-sigma ADCs in a nutshell, part 3: the digital/decimator filter

A digital-filter function attenuates the noise, and the decimator function slows the output data rate.
By Bonnie Baker -- EDN, 2/21/2008

Following the modulator in the delta-sigma ADC is a digital/decimator circuit. This circuit samples and filters the modulator stream of 1-bit codes. At the modulator output, high-frequency noise and high-speed sample rates are problems. However, because the signal now resides in the digital domain, you can apply a digital-filter function to attenuate the noise and a decimator function to slow the output data rate. Designers often intertwine the digital filter and decimator functions in the same silicon.

Figure 1 shows the signal as it travels through the digital/decimator-filter functions. The digital-filter function operates at the same rate as the modulator sampling rate (**Figure 1a**). Notice that the 24-bit code-train resembles the original signal (**reference 1** and **reference 2**). In the time domain, it looks like the digital-filter function is responsible for the low noise and high resolution of the delta-sigma converter. However, this function provides a second-order impact on the system noise by rejecting higher frequency noise, where the noise shaping from the modulator dominates noise reduction in the lower frequency band (**Figure 1b**).

The digital-filter function provides a digital version of the input, but the data rate is still too fast to be useful. Although it might appear that you have an abundance of high-quality, multibit samples at a high sampling rate, you don't need most of this data.

The second function of the digital/decimator filter is the decimator. Decimation is the process of reducing a digital signal's output rate to the system's Nyquist frequency. One simple way to implement a decimating function is to average together groups of 24-bit codes (**Figure 1c**). The decimator accumulates these high-resolution data words, averages several words together, outputs the average results, and dumps the data for the next average. A more economical way to implement a low-power decimator function is to simply pick out a 24-bit word every Kth sample without performing additional averaging. (K is equal to the oversampling or decimation ratio.)

Almost all delta-sigma converters incorporate a class of averaging filters called sinc or FIR filters, named for their frequency response. Many delta-sigma devices use other filters with sinc filters for two-stage decimation. Low-speed industrial **delta-sigma ADCs** usually use only a sinc filter.

In the frequency domain, you can see that this digital/decimator filter simply applies a lowpass filter to the signal (**Figure 1b**). In so doing, the digital/decimator filter has attenuated the higher frequency-modulator quantization noise. With the reduced quantization noise, the signal re-emerges in the time domain.

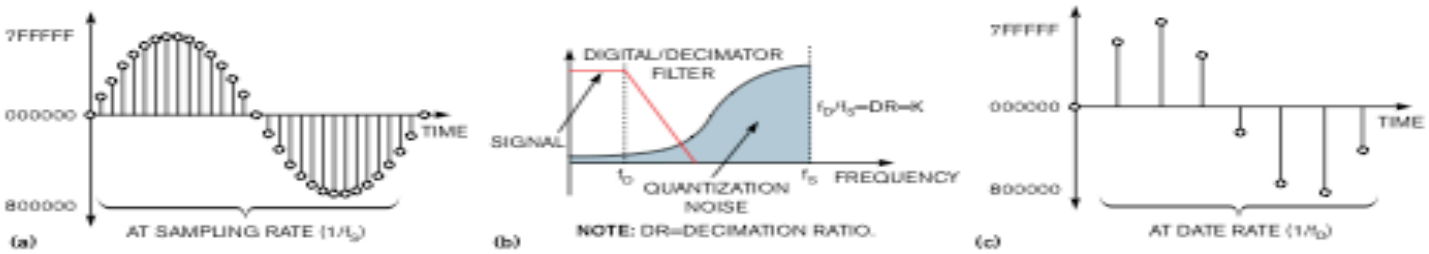

Figure 1 The digital-filter output function produces a high-resolution result (a), while rejecting high-frequency noise (b). The decimator function slows the output data rate (c).

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References

1. Baker, Bonnie, "**Delta-sigma ADCs in a nutshell**," *EDN*, Dec 14, 2007, pg 22.
2. Baker, Bonnie, "**Delta-sigma ADCs in a nutshell, part 2: the modulator**," *EDN*, Jan 2 pg 24.
3. Baker, R Jacob, *CMOS Mixed-Signal Circuit Design*, J Wiley & Sons, ISBN 0471227544.